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Millimeter-wave CMOS Transistor Design and Modelling: A Review

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Abstract

This paper presents an overview on the approaches and methodologies that were reported so far in modelling millimeter-wave CMOS active device. The paper begins by highlighting the limitations of the existing CMOS model provided by the foundry. Next, the performance metrics of millimeter-wave CMOS active device is described in brief. Then, the device modelling process for the active device which covers on the design of its test-structures, on-wafer measurement, device characterization and model generation were described. Finally, the current and future trends of mm-wave CMOS transistor are discussed. Device modelling or characterization is the first step involved in designing mm-wave CMOS circuit blocks thus accurate model for active device is required to ensure the success fullness in implementing the circuits.

Keywords: COMS transistor, device modelling

Introduction

The emergence of millimeter-wave (mm-wave) application has promoted research in both academic and industrial field towards the development of integrated circuit working in this spectrum. Mm-wave application which ranges from 30GHz to 300GHz has long been dominated by the III-V semiconductor group. Recently, with the availability of the unlicense 57GHz – 64GHz frequency spectrum, CMOS designer has the opportunity to venture into this frequency due to the rapid technology scaling of its gate length which leads to higher speed devices [1].

CMOS technology is well known in offering lower cost and higher level of integration compared to other technology such as Gallium Arsenide (GaAs) and Silicon Germanium (SiGe). However, implementing a mm-wave circuit using CMOS technology possess greater challenges compared to other technology since issues related to process variability and smaller breakdown voltages needs to be overcomed [2]. In order to address these issues, proper design methodology that includes careful modelling need to be taken into account when designing mm-wave CMOS circuit blocks.Modelling of mm-wave CMOS devices alone presents unique challenges

compared to its compound semicounductor counterpart due to the substrate's low resistivity, parasitic source, drain and gate resistance, and the relatively high loss tangent of its multi-layer dielectric [3].

Limitations of existing CMOS model provided by foundry

Designing a mm-wave CMOS circuit blocks require an accurate model of both its active and passive devices to ensure the circuit blocks can function properly as expected. Unlike the III-V technology such as GaAs which already has a matured library and model around the mm-wave frequency, CMOS technology is still considered new where the model for mm-wave CMOS is not readily available. Many of the previously reported mm-wave blocks show a significant deviation between the measurement and simulation results due to poor accuracy of its mm-wave model.

Typical CMOS transistor model provided by the foundry is usually meant for application less than 10GHz. This model which is also known as compact model enable designer to simulate their circuit without having to run expensive and time consuming experiment [4]. Heydari et al. had identified two reasons why the compact model is not suitable to be used in the mm-wave frequency [5]. The first reason is related to the parameter extraction process which is done in lower frequency. As mentioned earlier, since the compact model is only validated at low frequency, extrapolating the extraction data into mm-wave region may result in inaccuracy of the model. Apart from that, some device mechanisms such as the substrate network may not be captured well in low frequency thus making the model less robust in mm-wave frequency. The second reason is related to the layout of the transistor. In mm-wave frequency, the parasitic elements of the transistor's interconnection to the outside world have a large effect to the performance of the transistor. These parasitics are not included in the compact model since they are negligible at low frequency. This calls for a need in modeling the interconnect of the transistor and integrate it into the existing transistor model to make it feasible to be used in mm-wave frequency.

Performance Metrics of mm-wave CMOS Transistor

Having seen the limitations in using the existing CMOS model to work in mm-wave frequency, it is necessary for oneto custom design the transistor before it can be properly used in mm-wave circuit blocks simulation.One of the aimsin optimizing the transistor is to increase its unity current gain frequency (f_t)andmaximum oscillation frequency (f_{max}). f_t normally relates to the performance parameter of an analog circuitwhereby it indicates the product of gain and bandwidth of a single-stage amplifier. Maximizing $f_t$isusually beyond the control of a circuit designer since it is highly dependent on the process and technology of the foundry [6].f_{max}on the other hand captures the extrinsic parameter of the transistor, such as its parasitic gate resistance , thus it is more relevant and feasible for the circuit designer to address to. Minimizing the parasitic gate resistance is among the technique used to maximize f_{max}.The$f_t$andf_{max} can be estimated using the following equations [7]:

$$f_t = \frac{1}{2\pi} \cdot \frac{g_m}{C_{gs} + C_{gd}}$$

$$f_{max} = \frac{f_t}{2\sqrt{(R_g)(g_{ds} + 2\pi f_t C_{gd})}}$$

whereg_m is the transistor transconductance, C_{gs} is the gate to source capacitance, C_{gd} is the gate to drain capacitor, $R_g$is the gate resistance and g_{ds} is the output transconductance of the transistor. A representation of these parameters is

illustrated in a simplified small-signal model of a high-frequency CMOS transistor shown in Figure 1.

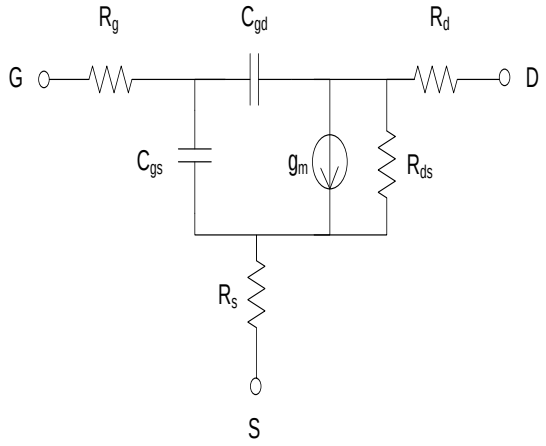


Figure 1: Simplified small-signal high-frequency model of a CMOS transistor

Another figure of merit that is commonly used to characterize a mm-wave transistor is the ratio of f_{max}/f_t. A high f_{max}/f_t ratio indicates a good or optimum design of a transistor, in terms of its layout design.

In designing active circuit blocks such as amplifiers to work at mm-wave frequency, it is important to study the gain and noise characteristic of the transistor first. Simulations such as maximum available gain (MAG), maximum stable gain (MSG) and minimum noise figure (NF_{min}) helps in identifying whether the transistor is suitable to operate at the desired operation frequency.

Design and Optimization of mm-wave CMOS Transistor

In general, device modelling process can be divided into four stages, which are the test-structure design, on-wafer measurement, device characterization and model generation.The work done in designing the test structure can be further grouped into two: modification of the conventional transistor layout and proposing a new layout structure.

Heydari et al. in their work had identified that $C_{gd}$and $R_g$of a transistor have the largest impact on f_{max} [5]. In their work, they had modified the existing compact NMOS structure to reduce the parasitic capacitance and resistance by changing the shape of the gate and drain to have smaller taper, increasing the number of gate and drain vias, and reducing the gate/drain overlap regions. The existing and improved NMOS layout is depicted in Figure 2. By addressing these two parasitic elements, they managed to achieve f_{max} for the improved structure up to 178GHz.

(a) (b)

Figure 2: Existing (a) and improved (b) layout of an90nm NMOS device [8]

Another work done involving optimization of the existing transistor layout structure is demonstrated by Chan et al. [7]. They focused on the interconnects of the transistor where they showed that changing the metal layers of the source, drain and gate interconnects can lead to reduction of the associated capacitive and resistive parasitics.By removing certain metal layers from the interconnects and using a ring-type gate topology, they managed get an $f_t$of 108GHz and f_{max} of 159GHz. Their existing and proposed layout structure is shown in Figure 3.Their analysis suggests that wiring effect will become more significant with increased number of finger and smaller width of each finger.Another important finding from their research work is that R_g is not the dominant parameter for $f_t$andf_{max}. Parasitic capacitance and resistance coming from the interconnects give more impact to both $f_t$andf_{max}.

Similar research work that focused on the extrinsic parasitic capacitance and resistance originated from the transistor's interconnect is presented in [9]. In this work, Jhon et al.studied the effects of additional parasitics caused by all metal layers connected with a single unit transistor from circuit-level perspective. The layout of the transistor was designed to be in a common-source configuration where the structure of the interconnects including metal wires from M1 to top metal layer, contacts and vias that were directly connected to other RF devices such as inductor or capacitor were analyzed.Three types of layout that they studied are shown in Figure 4. It is stated that in case of capacitive parasitics, it is suitable to focus on the extrinsic gate-to-drain capacitance (C_{gde}) compared to extrinsic gate-to-source capacitance (C_{gse}) since matching network is capable to cancel off the C_{gs}component. By reducing extrinsic$C_{gd}$and R_g components, they managed to achievef_{max} of 91GHz.

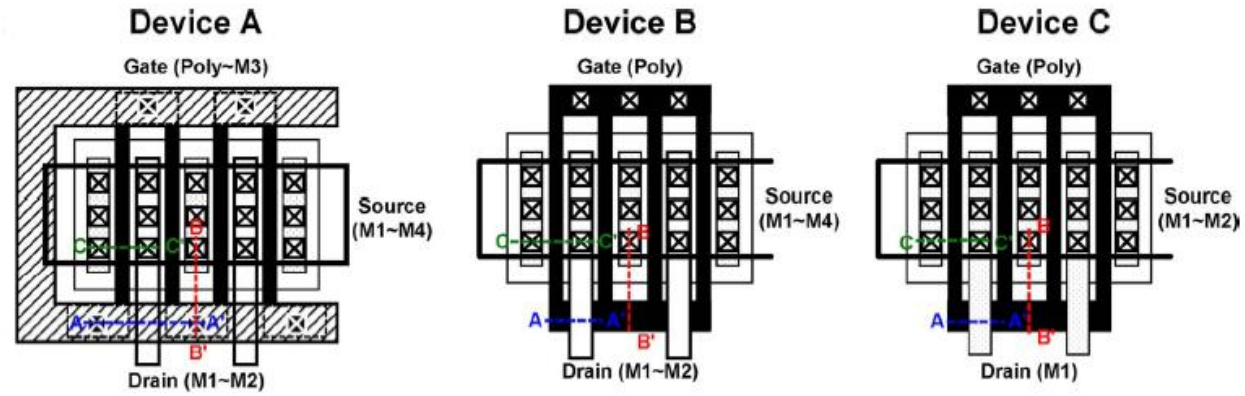


Figure 3: Existing (Device A) and proposed (Device B and C) layout for 65nm RF MOSFET [7]

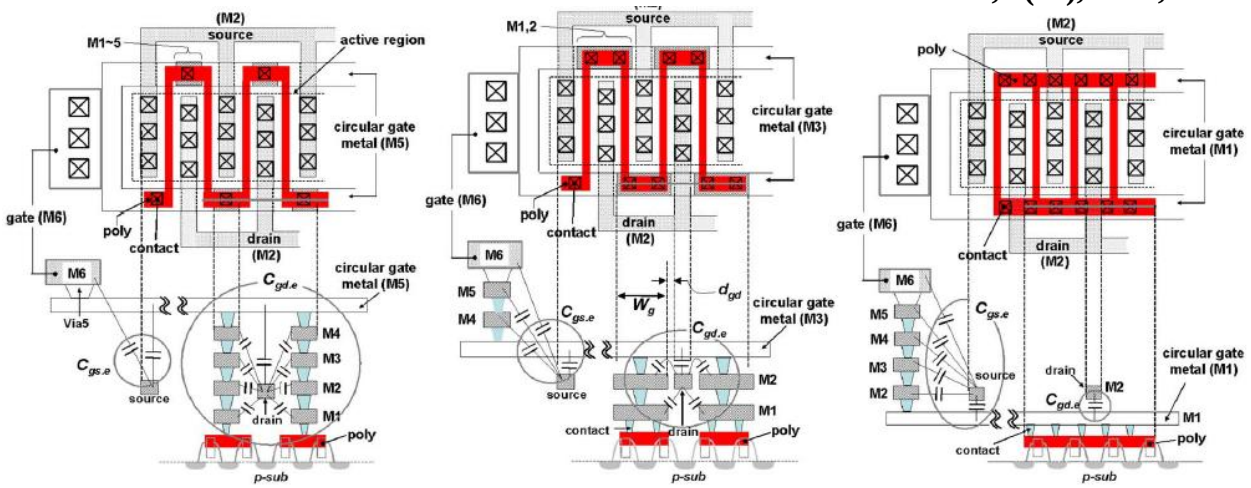


Figure 4: Three types of layout that were studied in [9]

Besides modifying the existing compact transistor model, Heydari et al. also proposed a new layout structure called the round-table structure to further improve the performance of the transistor [5]. They used a modular approach in their proposal where each unit cell (transistor) was connected in a matrix or circular form, as shown in Figure 5. The aim of this approach is again to reduce $C_{gd}$and $R_g$of the transistor. External double-contacts were used between the cells and multi-path connections were applied between sources and drain in the unit cell.Each unit cell too had double-gate contacts in order to decrease the resistance of the transistor's finger.Using this configuration, they manage to get f_{max} up to 300GHz.

A different layout structure for mm-wave active devices was proposed by Martineau et al. whereby the SOI CMOS transistor is divided into two equal parts with a double-contacted gate, as shown in Fig. 6 [10]. This is done to minimize gate resistance and parasitic capacitance while using co-planar waveguide (CPW) transmission line. In this structure, sources contacts are located on the transistor periphery to make it easier to contact to the CPW ground plane.Besides that, the structure also provides access for impedance matching towards and from the transistor to other components inside the circuit [11]. Their proposed structure managed to achieve an f_{max} of 194GHz.

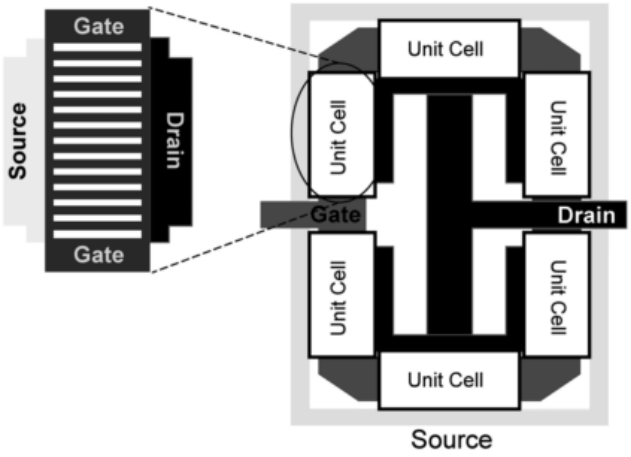


Figure 5: Conceptual picture of a round-table transistor proposed in [5]

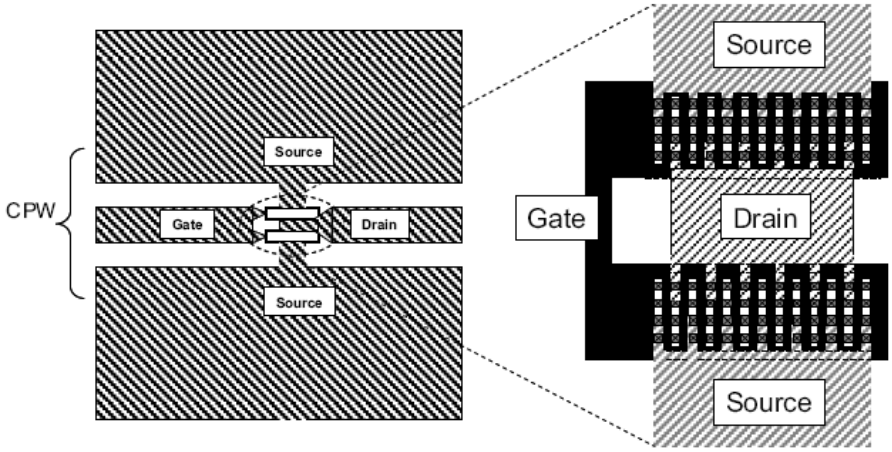


Figure 6: Structure of the transistor proposed in [10, 11]

In a more recent work, Liang and Razavi presented a layout structure that address specifically for differential pair transistor used in power amplifier (PA) [12]. Large multi-finger transistors are normally employed in PAs to handle large current. Highlighting the issue of output power and efficiency degradation causes by interconnects parasitics, Liang and Razavi proposed a layout technique for differential pair PA that considerably reduces the adverse effects of interconnect resistance and inductance on PAs performance.By quantifying the resistance and inductance in the source network, they proposed an interleaved layout technique that converts the source degeneration network seen by each transistor to a common-mode impedance. By applying this configuration, the source terminals carry only common-mode currents, omitting the interconnect parasitic from affecting the differential operation. Their proposed layout structure is depicted in Figure 7. Instead of using the normal f_{max} performance indicator, they evaluate their work based on the performance of an oscillator using conventional and the proposed transistors. Measured results showed thattheir proposed layout increases the output power from 5dBm to 10dBm and drain efficiency from 3.7% to 10.7%.

Measurement of mm-wave CMOS Transistor

Measurement of the test-structure is usually done using on-wafer measurement whereby the test chip normally consists of several configuration of width (*W),*length (*L*) and no. of finger (N_F) . The setup is similar to the normal RF measurement where it involves DC source measure unit (SMU), vector network analyzer (VNA) and GSG probe station and may also be integrated with parameter extraction software such as Agilent IC-CAP [3]. An example of the measurement test-setup is shown in Figure 8.

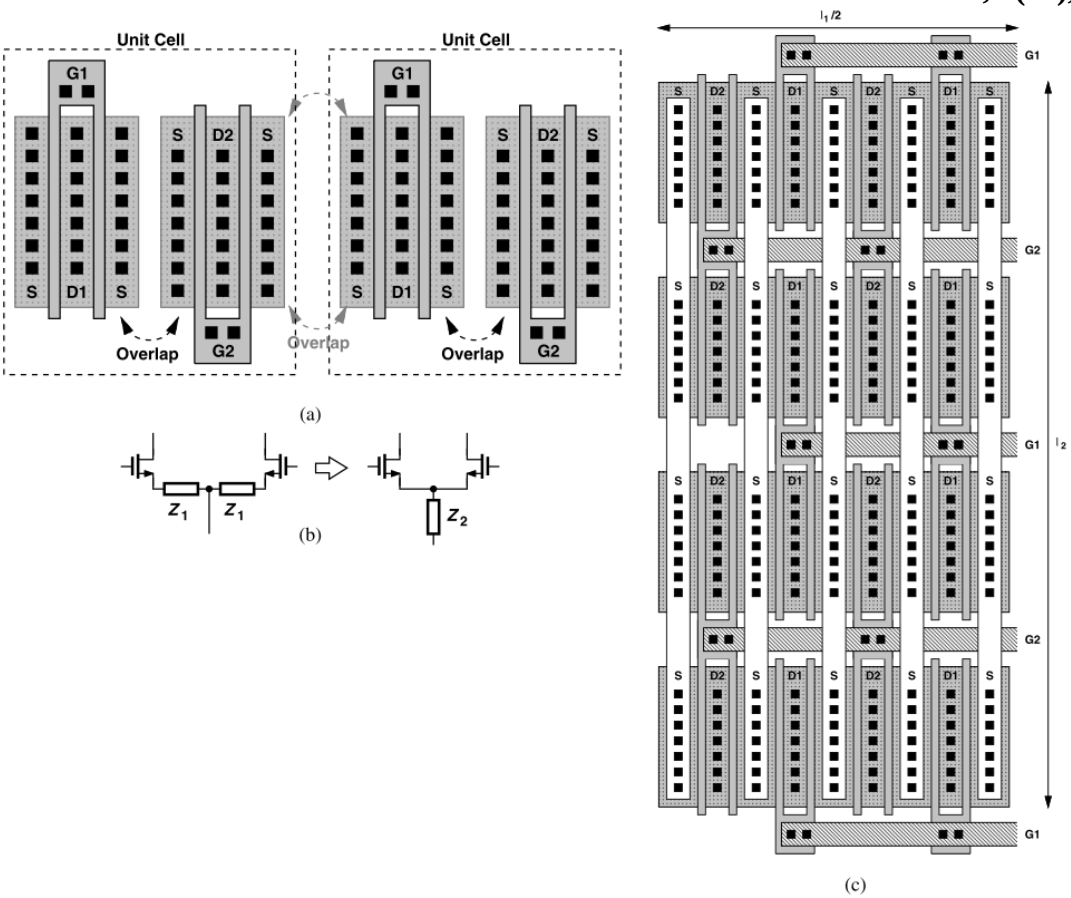


Figure 7: (a) Unit cells in proposed structure (b) Transformation of the degeneration impedance (c) Combined cells in a complete differential pair [12]

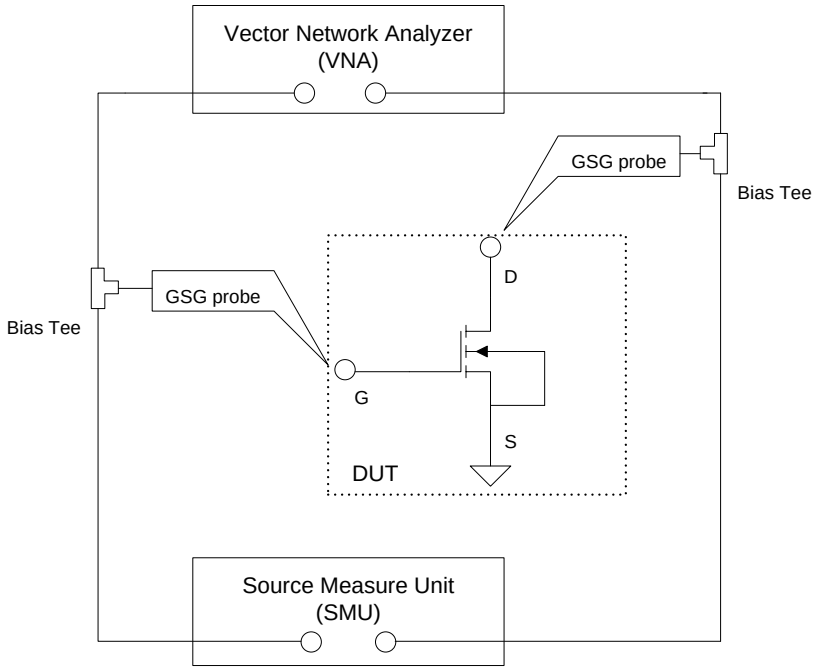


Figure 8: Test-setup for on-die transistor measurement

Different de-embedding techniques have been reported for mm-wave active device measurement. Jhon et al. used a two-step de-embedding process using open and short test structures pattern to remove on-wafer pad parasitics [9]. The extraction method from Y-parameter analysis was employed to determine the small-signal parameters of the devices.On the other hand, Shigematsu et al. used Line-Reflect-Line (LRL) calibrations to extract the S-parameters of the intrinsic transistor [13]. The test structures involved two lines of different lengths and an open structure where the device under test (DUT) consisted of an intrinsic transistor with outgoing electrode lines for the gate and drain. By using the technique, they were able to set the calibration reference planes to the edges of the outgoing lines and obtained the intrinsic S-parameters as shown in Figure 9.

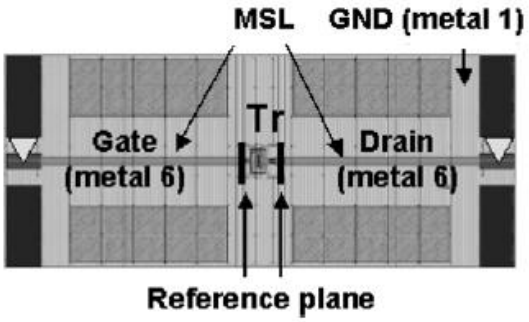


Figure 9: The DUT test-structure presented in [13]

Another work that uses open and short de-embedding method is demonstrated by Varonen et al. in [14].A CPW test-structure was designed for the transistor together with its open and short test-structures pattern. Besides extracting the S-parameter data, the noise behaviour of the transistor is also considered. The noise produced by the shunt admittance and series impedance of the test structures were substracted from the measured data using correlation matrix method.The technique is further elaborated in a separate literature in [15].Besides using the S-parameter related de-embedding techniques, transmission ABCD matrices can also be used to de-embed the pad and transmission line. This is used by Dawn et. al. in [16]. Their calibration test-structure pattern is shown in Figure 10.

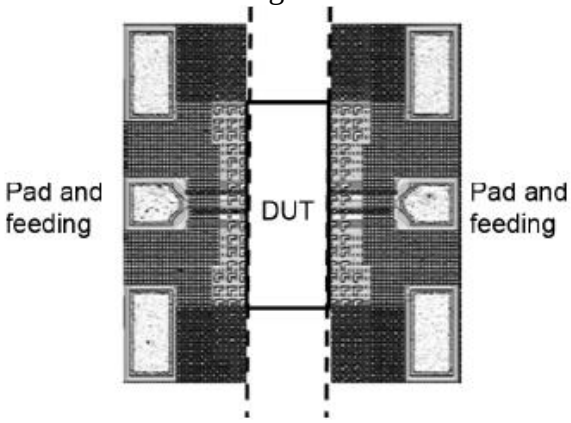


Figure 10: The calibration test-structure pattern presented in [16]

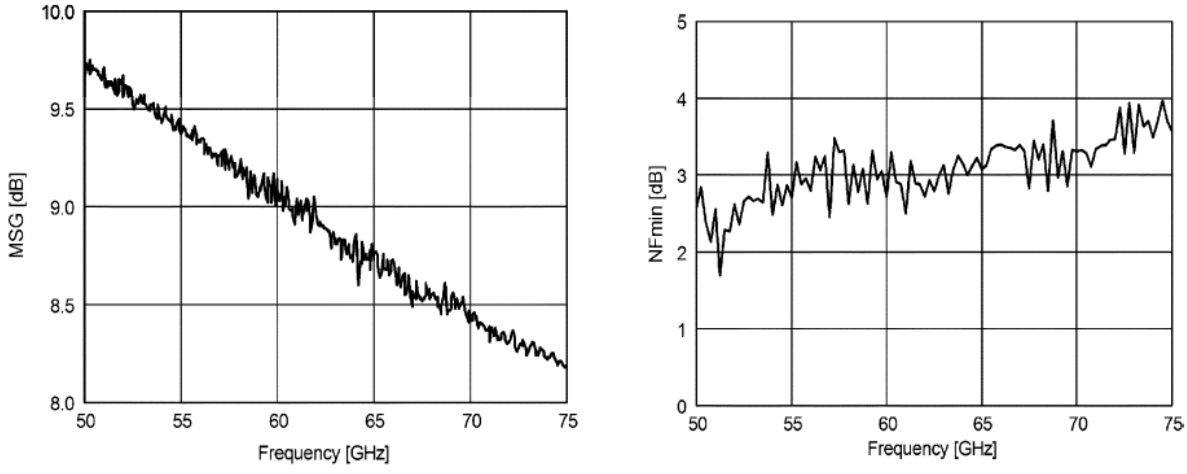
In [5], Heydari et al. claimed that the typical de-embedding step is a major source of inaccuracy at mm-wave frequency due to the imperfections of the de-embedding structures. Therefore, in oppose to the traditional de-embedding methods, they employed a model-based de-embedding approach which is called the recursive modelling technique in their measurement.Using this method, the pad and transmission line used in the test structure are modelled separately before they are embedded into the DUT. The probing pad was first modelled based on an equivalent circuit. It is then used to model the transmission line which is based on a physical lossy transmission line model where the complex characteristic impedance,Z_o, and the propagation constant, γ, were included.Finally both the pad and transmission line's model were embedded into the complete DUT. Overall, the modelling is done in steps where each resultaffects its next stage making it recursive in nature.

Characterization of mm-wave CMOS Transistor

During characterization, the transistors are analyzed by studying its DC I-V curve and S-parameter performances across different configuration of *W*,*L* and N_F.Other parameters such as f_t,f_{max}, f_{max}/f_t ratio, MAG and MSG may also be simulated at this stage. This is important since all the analysis will help in deciding the best configuration of transistor to be used in the circuits. As mentioned previously, the test chip normally consists of several configurations of*W*,*L* and N_F. However, due to time contraint and process complexity, not all of the configurationsmay be used in the modelling process. The best configuration of transistor that gives the desired performance, for example the highest MAG or MSG, will be used for device modelling.

Doan et al. determine the optimum finger width for a 0.13um CMOS process by fabricating and measuring multi-fingered common-source transistor with *W* varied from 1µm to 8µm and N_F varied from 40 to 100 [17]. Each transistor was analyze at different bias points, with I_{ds} varied form 20 to 300µA and V_{ds} fixed at 1.2V. It is found that reducing *W* from 2µm to 1µm led to an increment of f_{max} to 15%. Thus, 1µm was chosen as the optimum finger width for their device. Setting the transistor to have N_F=100, *W*=1µm and *L*=0.13µm, they managed to achieve an f_{max} of 135GHz, unilateral gain of 8.6dB and a MSG of 6.3dB at 60GHz.

A similar approach is presented by Varonen et al. where the selection of transistor to be used in their circuit came from a set of common-source transistors [14]. Based on the measurement of the transistors, the optimum transistor configuration chosen was *W*/*L* = 90µm/0.07µm. The transistor achieved an MSG of 9dB at 60GHz. In terms of noise performance, the NF_{min} achieved was around 3.0dB with I_{ds}andV_{ds} fixedat 18mA and 1.2V respectively. Figure 11 shows the measurement results on MSG and NF_{min} for the transistor. The transistor is used in their amplifier and mixer circuit design.



(a) (b)

Figure 11: Measured result on (a) MSG and (b) $NF_{min}$of the transistor with *W*/*L* = 90/0.07 presented in [14]

65nm Technology	Device A	Device B	Device C
Gate	Poly – M3	Poly	Poly
Source	M1 – M4	M1 – M4	M1 – M2
Drain	M1 – M2	M1 – M2	M1
C_{gs} (fF)	34.4	30.5	30.2
C_{gd} (fF)	16.1	13.0	12.7
C_{total} (fF)	50.5	43.5	42.9
I_{ds} (mA)	4.8	4.8	5.1
g_m (mS)	30.4	30.4	31.2
R_g (Ω)	3.68	4.02	4.33
f_t (GHz)	89	102	108
f_{max} (GHz)	130	155	159

Table 1: Summary of the parameter comparison presented in [7]

Characterization is also useful when it comes to comparing different layout design of transistors. In [7], three layout designs having a fixed size ofN_F=40, W=1µm and L=0.07µm with biasing of $V_{ds}$and V_{gs}equal to 1.2V and 0.7V respectively, were compared. The layouts of the three transistors are shown previously in Figure 3. By extracting their small-signal parameter together with the f_t and f_{max}, Chan et al. managed to make a fair comparison between the three devices quantitatively. The summary of the comparison is shown in Table 1. Similar trend is found in [9] where qualitative analysis involving the extracted small-signal parameters,f_t and f_{max}together with power gain is used to compare different transistor layouts.

Modelling of mm-wave CMOS Transistor

Developing an accurate model for the mm-wave CMOS transistor is important to ensure the circuit blocks can work well as expected. Modelling take place after the fabricated test structures are measured and characterized. A common practice to model microwave devices is by measuring its s-parameter and using the data as a black box. However, a drawback in using this technique is that the common s-parameter measurement is usually small-signal in nature. Thus, it is not suitable for non-linear and large signal devices such as mixer and power amplifier. Besides that, the measurement is usually fixed at specific bias point; therefore it is not convenient for the designer to further improve the circuit design in term of biasing.

A modelling methodology that utilizes this technique on top of a standard small-signal or BSIM3 model is demonstrated by Doan et al. in [18]. The models were extracted for fixed layout whereby the layout of the transistors in the circuit are identical to the one used for model extraction to guarantee its accurary. The core device is modelled using either a lumped small-signal model or using a standard BSIM3 model. The extrinsic component values and device parameters were extracted from the measurement data using a hybrid optimization algorithm in Agilent ICCAP. The resultant extended model is shown in Figure 12.A good broadband matching is obtained when the simulated model was compared to the measured data thus validating their proposed model.The same technique isalso highlighted by Heydari et al. in [5] where parasitic resisitance and inductance as well as substrate network were added to the hybrid-π model of the core transistor.

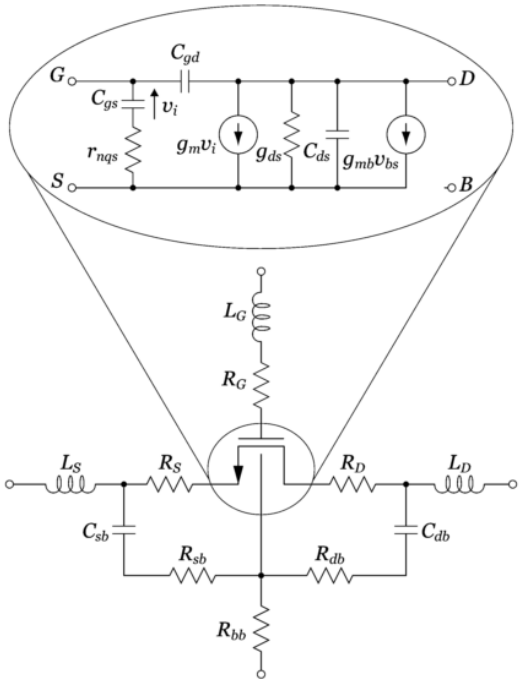


Figure 12: The extended CMOS transistor model proposed in [18]

Another measurement-based model was demonstrated in [16, 20] by Dawn et al. The group managed to incorporate scalable parameter in their model. Derived using Agilent ICCAP software, the single-model transistor, scalable in term of temperature, *T*and transistor width, *W*, was implemented using non-linear functions. The modeling process started with DC I-V characteristic and S-parameter measurement up to 65GHz across a temperature range of -25ºC to 80ºC. From the combination parameter of *T*and *W*, a core BSIM3 model was extracted using Agilent ICCAP. It is extracted at room temperature and was optimized to include model parameters as a function of *T* and *W*. During curve fitting process, the standard BSIM parameters were disable and replaced by external parameters as a function of *T* and *W*. The intrinsic BSIM3 parameters such as the channel drain-source capacitor (*cdsc*) was also extracted using the software and were derived as a function of *T* and *W*. The parasitic and model parameters were implemented in two-variable second-order polynomial functions. The model was proved to be valid since excellent matching was obtained against the measured S-parameter results.

Current and Future Trend of mm-wave CMOS Transistor

The approaches and methodologies that have been presented in this paper show that modelling of mm-wave CMOS active devices is still in its early stages with respect to the current phase of mm-wave technology development.CMOS technology is a promising candidate in mm-wave communication since prediction by the 2007 version of the International Technology Roadmap for Semiconductors (ITRS 2007) shows that the f_t of MOSFETs is expected to become greater than SiGe HBT by 2014, as shown in Figure 13 [21].

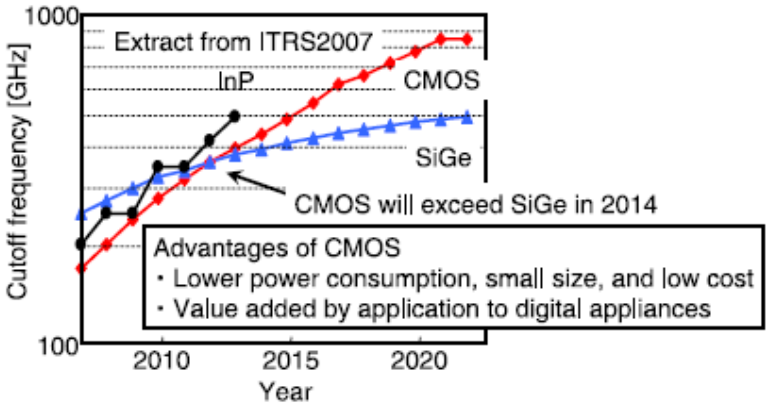


Figure 13: Chronological change in device performance as predicted by ITRS 2007 [21]

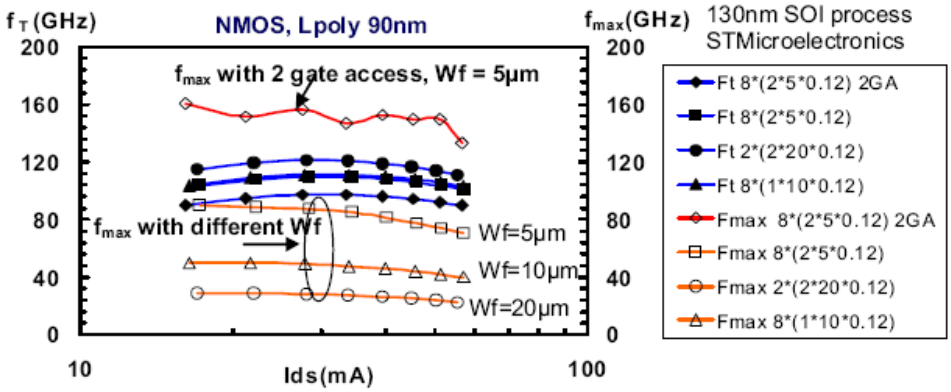


Figure 14: Influence of CMOS transistor layout over f_t and f_{max} described in [11]

At present, it is observed that in order to design a mm-wave CMOS circuit block, one must first start with the design of its active devices first since mm-wave CMOS model is not readily available from the foundry. It is obvious that most of the research done in designing the transistor aim in minimizing the extrinsic parasitic effect of the transistor to enable the transistor to work in mm-wave region.It is interesting to note that the optimum finger width, *W*, chosed for the transistor usually revolved around values less than 5µm [11, 22].A study on this trend showed that smaller *W* achieved higher f_t and f_{max} compared to larger *W*, as shown in Figure 14.

An encouring trend can also be seen in the modelling process since research work does not only focus on modelling fixed devices as scalable parameters are also included during modelling [16]. Another improvement done towards mm-wave CMOS transistor modelling is the inclusion of noise modelling and characterization [14, 23]. This is important since a robust transistor model should also include the noise behavioral of the transistor.

In the future, it expected that a more thorough research will be carried out in producing a complete mm-wave CMOS transistor model. To ensure the model can be used in designing various mm-wave CMOS circuit blocks, the model must be able to predict the small-signal and large-signal behavioral of the transistor together with the noise characteristic accurately. The sensitivity of the transistor towards the process-voltage-temperature (PVT) variation should also be considered.

Conclusion

CMOS technology has been identified as a promising candidate to boost millimeter-wave communication due to its proven performances. This article provides an overview on the approaches and methodologies in designing and modelling millimeter-wave CMOS active devices that are available in the literature at present. The paper first covers the limitations of the existing CMOS model provided by the foundry. This is followed by a brief description on the performance metrics of the millimeter-wave CMOS active device. Then, the device modelling process starting from the design of the transistor, on-wafer measurement, device characterization and model generation, from various research works are studied and compared. Finally, the current and future trends of mm-wave CMOS Transistor from the authors's perspective are highlighted.

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